UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,424	07/12/2002	Kwun-Yao Ho	9407-US-PA	9331

31561 7590 04/15/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,424	HO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1004//29 Oct 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed 19 January 2005. The Examiner acknowledges the amendments to Claims 1-5, 7 and 9. Claims 1-9 remain pending in the instant amended Application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites "a plurality of embedded patterned circuits, **each embedded patterned circuits comprising a plurality of patterned circuits embedded in a first dielectric layer**" (bold/underline emphasis added). What the bold/underline portion is trying to claim is unclear because the above-cited claim language may be construed as a multilayer structure within a single dielectric layer, or some special arrangement of distinct patterned circuits in a single dielectric layer (neither of which, by the way, are supported in the disclosure), or, a plurality of patterned circuits, each such patterned circuit embedded in a corresponding first dielectric layer, which does, indeed, have

support in the disclosure but is **not what the present claim language is reciting** with sufficient clarity for the Examiner to be sure as to whether or not this is, in fact, the aspect of the disclosed invention that the Applicant is trying to claim. Accordingly, the claim language should be further amended to be clear as to what is being claimed and to claim what the disclosure supports, thus removing the potentially new matter. For example, the above defective lines could be changed to *--a plurality of embedded patterned circuits, each embedded patterned circuit comprising a patterned circuit embedded in a corresponding one of a plurality of first dielectric layers--*. This recommended version (in italics) will be the interpretation taken by the Examiner for the purpose of reading prior art thereon or determining allowable subject matter.

Claim 5 recites "a plurality of second dielectric layers, **each** of the second dielectric layers has **a plurality of circuit layers**" (bold/underline emphasis added). Again, as in the discussion concerning Claim 1, above, the Examiner notes that the disclosure does not support a plurality of circuit layers in each of the second dielectric layers (i.e., either a multilayer structure or some special arrangement of distinct circuit layers within a single dielectric layer) of Claim 5; rather, there is supported in the disclosure a circuit layer in each of the second dielectric layers. No mention is made, or significance implied, to a **plurality** of circuit layers in a **single** dielectric layer in the Applicant's disclosure. Accordingly, the claim language should be further amended to be clear as to what is being claimed and to claim what the disclosure supports, thus removing the potentially new matter. For example, the above-cited defective lines could be changed to *--a plurality of second dielectric layers, each of the second dielectric*

layers having a circuit layer--. This recommended version (in italics) will be the interpretation taken by the Examiner for the purpose of reading prior art thereon or determining allowable subject matter.

Claims 2-4 depend from base Claim 1, and Claims 6-9 depend from base Claim 5, and therefore inherit the defects of the respective base claims.

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Kurita et al. (US 6,583,364 B1)** Frankeny et al. (US 5,146,674)*

Gerber et al. (US 5,401,913) Frankeny et al. (US 5,121,299)*

*Already made of record by the Examiner in the previous Office Action of October 20, 2004.

**Corresponds to CN 1290033 A, already made of record in Applicant's IDS filed October 29, 2004 (Paper No. 1004).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Gerber et al.

As to Claim 5, Gerber et al. discloses, in Figs. 9 and 10: a plurality of first dielectric layers 10, 26, 28, 30 and 32 (col.3: 68-col.4: 1, col.5: 46-49 and col.6: 4-6), each of the first dielectric layers having a plurality of via studs: i.e., studs 20 in first dielectric layer 10, studs 42 in first dielectric layer 26, studs 44 in first dielectric layer 28, studs 46 in first dielectric layer 30 and studs 48 in first dielectric layer 32 (the via studs are made of via metal, as disclosed in col.4: 66-col.5: 8 and claim 7 in col.8: 58-59; also, there are plural via studs in each of the above-cited first dielectric layers as disclosed in col.4: 42-44 and 63-66, and in col.6: 58-67); a plurality of second dielectric layers 24, 58, 60 and 62 (col.5: 58-63), each of the second dielectric layers 24, 58, 60 and 62 having a circuit layer 36, 16, 38 and 40, respectively (i.e., after lamination, the final multilayer product is formed wherein each of the second dielectric layers 24, 58, 60 and 62 has a circuit layer 36, 16, 38 and 40, respectively, embedded therein, as shown in Fig. 10, and the individual traces and contacts of a circuit layer are thereby electrically isolated by the respective second dielectric layer, as disclosed in col.6: 12-21); the second dielectric layers 24, 58, 60 and 62 are laminated to the first dielectric layers 10, 26, 28, 30 and 32 and the circuit layers 36, 16, 38 and 40 are electrically coupled to each other through the via studs 20, 42, 44, 46 and 48 (Fig. 10; col.6: 12-21), wherein the via studs 42 and 48 in two most exterior dielectric layers 26 and 32, respectively, are used as a plurality of solder pads directly (Fig. 10; col.5: 15-27 and note via cover layers 50 and 56, disclosed in col.5: 52-55, are the same solder layer as via cover layer 22 described in col.5: 15-27).

As to Claim 6, Gerber et al. further discloses that a pattern of the circuit layers is designed as landless; i.e., each circuit layer 36, 16, 38 and 40 is a trace metal layer that include contact portions that act as "pads" for contacting the via metal of via studs 20, 42, 44 and 48 of the respective first dielectric layers; col.5: 8-10. Accordingly, as taught by Gerber et al., there are no lands on circuit layers 36, 16, 38 and 40 that constitute the large-area via lands of the prior art that limit component density on the circuit board, as taught by Gerber et al. in col.1: 58-62).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita et al.

A) As to Claim 1:

I. Kurita et al. discloses, in the embodiment of Figs. 8a and 8b: a plurality of embedded patterned circuits, each embedded patterned circuit comprising a patterned circuit (one of patterned circuits 16 and 86_1) embedded in a corresponding one of a plurality of first dielectric layers 17 and 89_1, respectively; a plurality of via stud layers, each via stud layer respectively comprising a plurality of via studs 84_1 and a plurality of via studs 84_2 (col.7: 13-15), encompassed by a respective second dielectric layer 87_1 and 87_2, wherein tops of each of via studs 84_1 and 84_2 are protruded from one surface of the second dielectric layers 87_1 and 87_2, respectively; the embedded patterned circuits 16 and 86_1 in first dielectric layers 17 and 89_1, and the via stud layers in second dielectric layers 87_1 and 87_2 (Figs. 8a and 8b) are laminated together such that at least some of the via studs 84_1 and 84_2 are aligned and contacted directly with some of the embedded circuits 16 and 86_1.

II. In the embodiment of Figs. 8a and 8b, Kurita et al. further discloses, in the substrate 42, a plurality of third dielectric layers 12 and 89_2 (Fig. 8b) but does not disclose that third dielectric layers 12 and 89_2 each have a plurality of via openings therein.

III. In the embodiments of Figs. 13a,b and 14a,b, Kurita et al. teaches that the multilayer structure can be further modified by the addition of via openings in each of a plurality of dielectric layers; i.e., the outermost dielectric layers, for the purpose of

expanding the number of layers of the substrate to form a multilayer circuit structure and for enabling the mounting of electronic components, such as semiconductor devices, on the multilayer circuit structure (col.15: 1-18 and col.17: 40-64).

IV. Since the embodiment of Figs. 8a,b have third (outermost) dielectric layers 12 and 89_2, and the embodiments of Figs. 13a,b and 14a,b teach that the outermost dielectric layers may be modified to include via openings, thus forming via opening layers that enable the addition of new substrate layers to form multilayer structures that increase the circuit density and functionality of the substrate and that further enable the mounting of electronic components, such as semiconductor devices to perform various electronic functions required by the application, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the third (outermost) dielectric layers 12 and 89_2 in the embodiment of Figs. 8a,b of Kurita et al. by forming via openings in each of the third dielectric layers 12 and 89_2 in order to use via studs to enable further expansion of the substrate 42 into a multilayer circuit structure with a higher density of circuitry and to further enable the mounting of electronic components thereon, thus providing a substrate with a greater functionality that meets the needs of an electronics application, as taught in the embodiments of Figs. 13a,b and 14a,b of Kurita et al.

B) As to Claim 2, Kurita et al. further discloses two via opening layers 12 and 89_2, arranged as two most exterior dielectric layers of the laminated substrate structure (already established in the rejection of base Claim 1, above).

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurita et al., as applied to Claim 2, above, and further in view of Frankeny et al. (US 5,146,674 and US 5,121,299).

I. Kurita et al. teaches that the via opening layer 110 (Figs. 13b and 14b) and 89_2 (Fig. 8b) may be any one of a variety of conventional resin materials (col.11: 4-9) and further teaches that the via openings are also used to mount semiconductor devices by solder interconnection, wherein the circuit and component interconnections through the via openings are solder interconnections (col.15: 1-7 and 16-19).

II. Kurita et al. does not teach that the via opening resin layer is a solder mask layer having said via openings. Kurita et al.

III. Frankeny et al. (US 5,146,674) discloses, in Fig. 24, a multilayer circuit structure with via studs 17 and 57 in via stud layers and teaches a semiconductor device 63 solder-mounted to via studs 57 with a via opening layer 61 that functions as a solder stop layer (col.8: 22-38) wherein the (then) co-pending US Application 07/459,087 (Frankeny et al.), now US 5,121,299, incorporated by reference (col.8: 36-38 and col.1: 15-22) teaches that the solder stop layer is a solder mask (see US 5,121,299: solder mask 26 in Fig. 13 and col.4: 27-34).

IV. Since both Kurita et al. and Frankeny et al. are both in the art of forming electronic packages having multilayer structures, to which, semiconductor components are solder-mounted, then the use of a solder mask to control the spread and shape of the solder joint taught by Frankeny et al. in above-cited US patents '674 and '299 would have been readily recognized as an effective control of the solder-mounting process of

the semiconductor component to the multilayer circuit structure through the via openings, ensuring reliable solder interconnect structures in the pertinent art of Kurita et al.

V. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to modify the third dielectric (resin) layer (either one or both of via opening layers 12 and 89_2) to be a solder mask layer, as taught by Frankeny et al., for the purpose of optimizing the solder-mounting process, wherein the solder joint formation between the semiconductor component and the multilayer circuit structure of the substrate is controlled to prevent solder spread and enhance good joint formation, thus ensuring reliable solder interconnect structures for the semiconductor components mounted on the multilayer substrate of Kurita et al., as taught by Frankeny et al.

Allowable Subject Matter

11. Claims 3 and 7-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. Applicant's arguments with respect to claims 1 and 5, as amended, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Kurita et al. (US 6,729,022 B2) discloses a multilayer circuit having embedded circuit layers 27, 28 and via stud layers 16, 18 (Fig. 5h). [This US patent corresponds to CN 1286591 A already made of record in Applicant's IDS filed October 29, 2004 as Paper No. 1004].

b) Odaira et al. (US 5,600,103) discloses an interconnect circuit comprising via studs 2 and 2' (Figs. 9A,B). [This US patent corresponds to CN 1053785 C already made of record in Applicant's IDS filed October 29, 2004 as Paper No. 1004].

c) Hino et al. (US 5,374,469) discloses a multilayer substrate with embedded circuit layers and via stud layers (Figs. 9 and 10).

d) Tsukamoto et al. (US 5,406,459) discloses, in Figs. 9A,B, via stud layers 44a and 49b.

e) Daigle et al. (US 5,046,238) discloses a multilayer circuit structure wherein each layer comprises via studs and embedded circuits (Fig. 6).

f) Obata et al. (US 6,812,412 B2) discloses a multilayer circuit structure comprising via stud layers 11 (Figs. 1 and 2).

g) Jiang et al. (US 6,163,957) discloses a multilayer circuit structure comprising via stud layers (Figs. 7-9).

h) Iijima et al. (US 6,828,669 B2) discloses an outermost via opening layer 210 for exposing via studs 208 to which semiconductor chip 205 is solder-mounted (Fig. 3 and col.9: 5-17).

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
April 13, 2005